Analysis of Drain Induced Barrier Lowering and Threshold Voltage in Sub-100 nm Silicon Nano-Wire Gate All Around MOSFET using High-K Gate Dielectric

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***Abstract*— Regular advances in short channel devices have made these devices appropriate for current chip architectures. Multi gate MOSFETs have proven to be a superior solution than traditional MOSFETs to reduce short channel effects and for the further miniaturization of transistor device in the nano-scale region. In the range of Multi Gate MOSFET, the Gate All Around MOSFET has been determined to be the most efficient for this task. Here the electrical analysis of silicon nano wire Gate all around MOSFET is reported with the perspective of short channel effects' efficacy. The Threshold Voltage Roll-off and Drain Induced Barrier Lowering effect has been explored in Gate-All-Around transistor with channel lengths in the sub-100 nm range, and an attempt has been made to explain the results from the energy profile of the device. The implementation and three-dimensional analysis of all transistor designs has been done utilizing TCAD.**

Keywords—drain induced barrier lowering, threshold voltage, energy barrier, gate all around MOSFET

I. Introduction

Today's electronic market is heading towards very complicated and high-speed electronic chips. This market force is pushing the electronic devices towards everlasting scaling. Device scaling delivers better switching speed and lower power consumption to the transistors. As a result of this, the chip density of the electronic system improves, allowing the chips to accept more sophisticated designs [1]. As the transistors enter the short channel region, due to the influence of this scaling, some unwanted effects start to affect the ideal transistor action. These adverse consequences are called short channel effects [2].

Due to the rigorous scaling, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have shrunk down to the sub-100 nanometer range from their initial size of 10 µm in the year 1971 [3]. At such a tiny dimension, it becomes impossible to overlook the short channel effects (SCE) of the transistor. For this reason, researchers keep trying to control these detrimental effects by making amendments in the classic MOSFET architecture.

When the distance between the source and the drain in an extremely small MOSFET transistor is on the order of the thickness of the depletion layer generated between the drain and the substrate, the device is said to be a short channel device. The effect of scaling in MOSFET leads to a number of short channel effects in these devices [4]. Out of them, the Drain Induced Barrier Lowering (DIBL) and Threshold Voltage Roll-off have been investigated prominently in this work.

In the short channel range of device dimensions, the drain potential has a very harmful effect on the channel region, which affects the MOS capacitor operation. This phenomenon is termed as the DIBL effect. This mechanism is quite similar to the punch through effect. MOSFET provides a potential barrier in the lack of a route for the charge carriers from source to drain in the week inversion region of operation [5]. Ideally this barrier should remain dispersed with drain potential as happens in the case of long channel MOSFET, but in the case of short channel MOSFET, the drain potential starts effecting this barrier. If a significant voltage is supplied to the drain electrode, it reduces the effective height of the potential barrier. The DIBL parameter is used to represent the intensity of this barrier suppression. It is described as the change in threshold voltage against the applied drain potential. Basically, the DIBL value indicates the struggle between gate and drain to control the channel region. A high DIBL value indicates low control of the gate in the channel area, which proves it, to be an unfavorable parameter for device performance. For this reason, researchers have been trying to inhibit the DIBL from time to time. These efforts have paved the way for continuous device scaling.

For the past several decades, researchers have been trying to suppress the short channel effect. These efforts have paved the way for continuous device scaling. After 2007, it was realized that it would be practically hard to continue scaling with planar bulk MOSFET architecture[6]. For this reason, high-K dielectric materials , metal gates, buried oxides, and other modest improvements have been exploited by the research community to produce transistor topologies that alleviate the challenges faced by scaling [7]. In this series of improvements, the multi-gate transistors were invented. Multi-gate transistors work on a general theory that with multiple gates, the gate-channel capacitance becomes two, three or four times bigger than what it usually is in conventional MOSFET. As a result, the control of the gate on the channel region is improved [8].

In the family of multi gate MOSFETs, the Gate All Around MOSFET (GAA-MOSFET) is the frontrunner in this performance. In GAA-MOSFET, the channel region is

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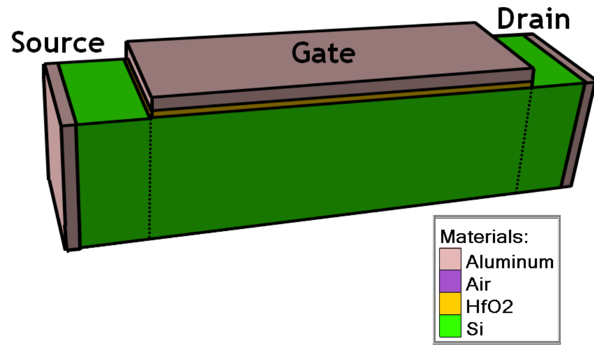

Fig. 1. Device architecture of Single Gate MOSFET

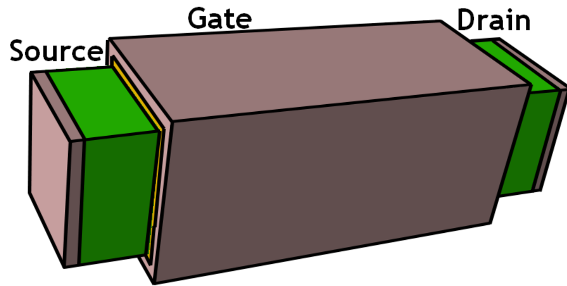

Fig. 2. Device architecture of Gate All Around MOSFET.

covered from all four sides by gate electrodes (figure 2). Tight gate-channel couplings from all four directions decrease short channel effects. Due to this fact, the DIBL, threshold voltage roll off and other SCEs are less prominent in these devices as compared to single gate MOSFETs.

II. Device Design and Simulation Framework

In this work, nanoscale GAA-MOS has been examined largely, using simulations. The simulated device architectures are displayed in figure 1 and 2. The gate region of a GAA-MOSFET covers the substrate region on all four sides (figure 2), whereas the gate region of a single gate MOSFET is found over the top of channel region only (figure 1).

All the device architects are implemented in the nano scale dimensions range. Here HfO_2 material is employed for the separation of channel area from gate, which possess higher dielectric constant than ordinary SiO_2 material. it is well-known that the usage of HfO_2 not only helps to extend oxide scaling restriction but also has many other advantages like reduced gate leakage, fewer short channel effect etc. [9], [10]. In all MOS architectures, the thickness of the gate to channel isolation has been retained at 1 nm. This thickness of oxide may get disturbed from its true physical dimension in case of polysilicon gate. When a polysilicon gate is employed in a MOS, a dielectric layer is generated at the gate to oxide interface, the thickness of which relies on the potential profile of the material and electrode [11]. At nano size, even such tiny layer influences the performance of the transistor. For this reason, metal electrodes have been utilized here for transistor designs. The thickness of the gate electrode has been fixed at 2 nm in all the architectures. The cross-section dimension of the substrate region is 20x20 nm, while its length is kept variable for the analytical purpose. Conventional silicon (Si)

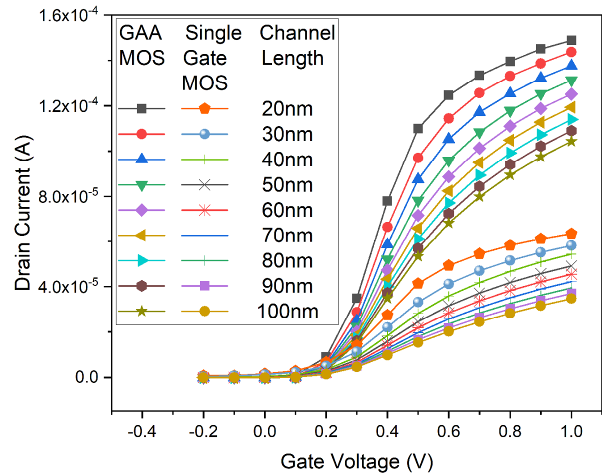

Fig. 3. Transfer Characteristics of Single Gate MOSFET and GAA-MOSFET at different channel length and V_D=0.1V.

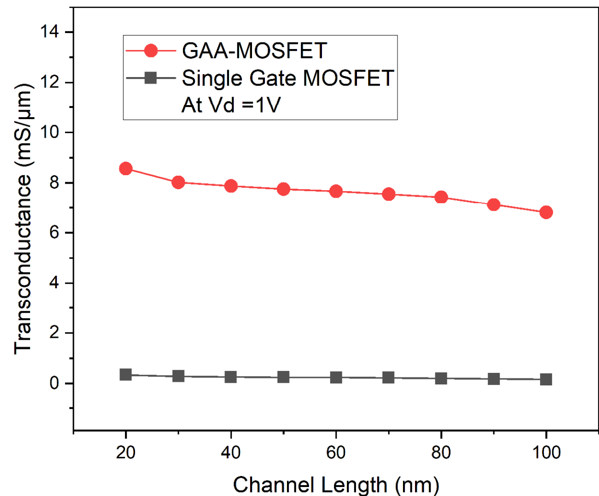

Fig. 4. Transconductance of Single Gate MOSFET and GAA-MOSFET at different channel lengths.

material has been employed to implement this region. The lengths of the source and drain resistive regions which are attached to both side of substrate region are preserved at 10 nm apiece. Conventional aluminum metal has been employed to implement the gate, source and drain electrodes in all device geometries. A donor type doping concentration of $1x10^{18}cm^{-3}$ has been employed in the source and drain resistive region, while the substrate region is maintained undoped for improved performance of the device.

Classical models are effective for replicating the electrical behavior of long channel bulk MOSFET. However, quantum mechanical models are useful for precise simulations of nanoscopic transistor devices. That is why the Schrodinger-Poisson model has been employed in all simulations, to model quantum confinement effects in an appropriate manner.

III. Simulation and Results

The purpose of this effort is to explore the transistor architectures affected by scaling. A primary effect of the scaling comes in the form of increased device performance. This can be understood from the on characteristics of the

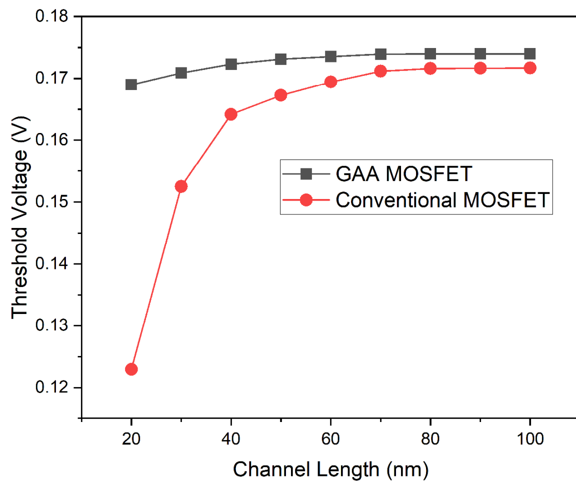

Fig. 5. Threshold Voltage of Single Gate MOSFET and GAA-MOSFET at different channel lengths.

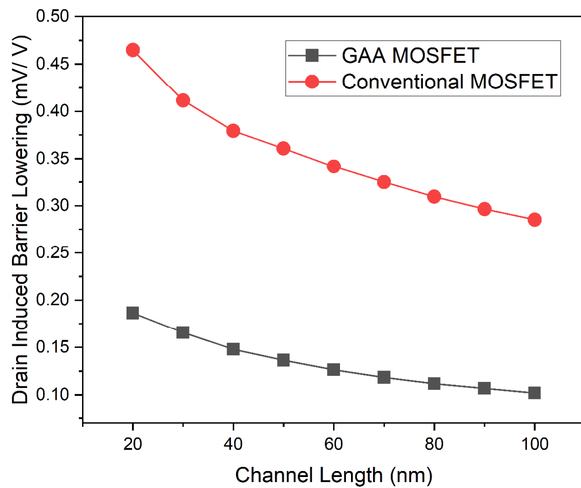

Fig. 6. Drain Induced Barrier Lowering of Single Gate MOSFET and GAA-MOSFET at different channel lengths.

device. The figure 3 displays the transfer characteristics of conventional MOS and GAA-MOS transistors. It is shown here that quadruple gate MOSFET delivers higher on-current values as compared to typical single gate MOSFET. On a scale of channel length of 60 nm size, this improvement is measured to be 174.97%. Apart from this, it can also be claimed that the ON current of the transistor device increases with the scaling of the channel length. Based on all computations, this increase in GAA MOSFET was identified to be 42.5% for a channel length sweep of 100 nm to 20 nm. This increase in transistor current with channel scaling can be explained by the enhancement in the device's transconductance.

Transconductance is an important attribute of device performance. The figure 4 displays the variation of the transconductance of the transistor devices with the channel length. The transconductance value illustrates how responsive the device is, to the applied gate potential. Here the GAA-MOSFET demonstrates 8.17 mS/μm higher transconductance than the single gate MOSFET at 20 nm channel length (figure 4). Apart from this, this improvement roughly has been determined to be 8.22 mS/μm when the channel length is

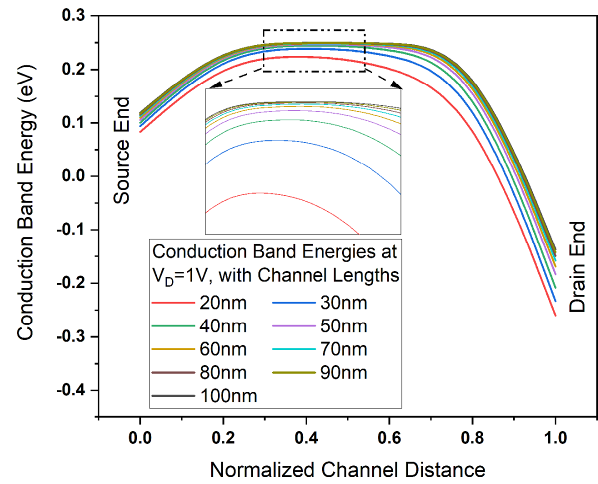

Fig. 7. Conduction Band Lower Edge Energies at the top of the channel below top gate of GAA-MOSFET at different channel lengths against normalized channel at V_D=1V.

scaled from 100 to 20 nm in GAA-MOSFET, against a marginal improvement of 0.17 mS/μm in its conventional counterpart with same channel length scaling values.

All the performance improvements realized with scaling, come with the penalty of SCEs. The SCEs lead the transistor towards non-ideal behavior. The threshold voltage roll-off is one of the key effects of all these. The threshold voltage of the transistor is changed due to the threshold voltage roll-off effect. The figure 5 demonstrates the dip of threshold voltage with channel length scaling in both the devices. Here it could be said that there is a threshold voltage drop in both the transistors with decreasing channel length, although in single gate MOSFET it is noticed substantially larger than in GAA MOSFET. This observation implies that GAA-MOSFET is more immune against threshold voltage roll-off, than single gate MOSFET.

DIBL is a significant short channel effect that, as its name suggests, refers to the decrease of the barrier of the substrate region by the drain applied voltage. The figure 6 illustrates the DIBL values of both the transistors with the variation of channel length. Here it appears that the DIBL values observed in a single gate MOSFET at all channel lengths are substantially greater than the DIBL values for GAA-MOSFET. The GAA-MOS demonstrates a maximum of 149.65 % significant improvement over the single gate MOSFET, observed at 20 nm of channel length node. In both the MOSFETs, it is noticed that the DIBL values rise with decreasing channel length, although the increase in GAA-MOSFET is less noticeable as compared to the single gate MOSFET. Both these observations suggest that the quadruple gate architecture in the nano scale region provides higher resilience to the device against DIBL.

The increment of the DIBL exhibited in the MOSFET with the decrement of channel length can be understood from the energy profile of the device. The figure 7 illustrates the state of the conduction band lower edge on the silicon surface at the oxide-Si channel interface below the top gate of the GAA-MOSFET. It can be seen here that with decreasing channel length, the barrier existing between the source and drain diminishes. Due to this impact, it can be understood that with decreasing channel length, the DIBL effect becomes stronger.

IV. Conclusion

The performance of single gate MOSFET and GAA MOSFET with high-k dielectric gate insulation, at nano scale dimensions were examined by extensive simulations and the functional superiority of GAA-MOSFET was validated. It has been shown that GAA-MOSFET shows a remarkable transconductance boost of 8.17 mS/µm than single gate MOSFET, which further results in an improvement of 174.97% in ON current. These perks related to scaling in the nanoscale region also bring together the adverse short channel effects. The performance of conventional MOSFETs and GAA-MOSFETs against short channel effects was analyzed, and it was shown that GAA-MOSFET which not only shows significantly better device performance than the conventional MOSFET, also exhibits superior immunity against crucial short channel effects like the threshold voltage roll-off and DIBL effect.

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